Notice of Allowability	Application No.	Applicant(s)	
	10/657,137	OHTANI, HISASHI	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Request for Continuing Examination (RCE) filed May 12, 2005.*.

2. ☒ The allowed claim(s) is/are *40-71*.

3. ☒ The drawings filed on *09 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 5-12-05 & 6-07-05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Michael Trinh
Primary Examiner
Act SPE

DETAILED ACTION

This Office Action is in response to the Request for Continuing Examination (RCE) filed May 12, 2005.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Hayden on August 3, 2005.

The **claims** in the application has been amended as follows:

40. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the CPU comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a thickness of the first gate insulating film is smaller than that of the second gate insulating film.

43. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the CPU comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a thickness of the first gate insulating film is 80% or less of that of the second gate insulating film.

46. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the CPU comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a width of the first gate electrode is smaller than that of the second gate electrode.

49. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the CPU comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a width of the first gate electrode is 80% or less of that of the second gate electrode.

52. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the memory comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a thickness of the first gate insulating film is smaller than that of the second gate insulating film.

55. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the memory comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a thickness of the first gate insulating film is 80% or less of that of the second gate insulating film.

58. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the memory comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a width of the first gate electrode is smaller than that of the second gate electrode.

61. (Currently Amended) A display system comprising:

a CPU formed over a substrate;

a memory connected to the CPU;

an X-Y branch connected to the CPU;

a column driver connected to the X-Y branch;

a **[[low]]** row driver connected to the X-Y branch; and

an active matrix circuit connected to the column driver and the **[[low]]** row driver,

wherein the memory comprises a first semiconductor layer, a first gate insulating film on the first semiconductor layer, and a first gate electrode on the first gate insulating film,

wherein the active matrix circuit comprises a second semiconductor layer different from the first semiconductor layer, a second gate insulating film on the second semiconductor layer, and **[[the]]** a second gate electrode formed on the second gate insulating film,

wherein a width of the first gate electrode is 80% or less of that of the second gate electrode.

64. (New) A display system according to claim 40, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

65. (New) A display system according to claim 43, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

66. (New) A display system according to claim 46, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

67. (New) A display system according to claim 49, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

68. (New) A display system according to claim 52, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

69. (New) A display system according to claim 55, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

70. (New) A display system according to claim 58, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

71. (New) A display system according to claim 61, wherein the first semiconductor layer and the second semiconductor layer are formed from a common semiconductor layer.

Allowable Subject Matter

Claims 40-71 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to display systems:

Hotto (5,444,457)	Nakano (5,191,373)
Nelson et al. (5,113,511)	Page et al. (6,078,316).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Trinh
Primary Examiner
Act SPE

IMS
July 23, 2005